Modeling of a Low Voltage Cross-Coupled Oscillator

Rodrigo Giordano Ono
Division of Design, Analysis and Qualification of Electronic Circuits
CTI Renato Archer
Campinas, Brasil
rgono@cti.gov.br

Antonio Carlos da Costa Telles
Division of Design, Analysis and Qualification of Electronic Circuits
CTI Renato Archer
Campinas, Brasil
actelles@cti.gov.br

***Abstract* - This work presents the analysis of the special case of the low-voltage cross-coupled oscillator, when the transistors act as ideal switches. A theoretical model to the oscillation frequency is presented and compared with that of an experimental circuit, showing very good agreement.**

I. Introduction

Cross-coupled oscillators are very useful circuits, with broad application on RF field [1]. The typical circuit includes a bias current at the sources of the transistors. The classical approach to the analysis is as a linear circuit [1]. However, like all other oscillators, the cross-coupled oscillator is a nonlinear circuit.

Buonomo & Lo Schiavo analyzed the circuit as a VCO. Varactors were responsible by the frequency tuning [2], [3]. All nonlinearities were included, and the approach used a combination of the Poincaré-Lindstedt and harmonic balance methods developed by Buonomo & Di Bello [4].

The inclusion of the bias current source demands the operation at higher voltages. In some applications, however, this level of voltage is not available, such as those powered by single photovoltaic cells.

A few authors analyzed the oscillator without a bias current source. Ge *et al.* [5] discuss the behavior or the circuit with a third order nonlinearity. Daliri & Maymandi-Nejad [6] present a model for a more generic circuit. They consider that the output voltages are equal, shifted each other by 180 degrees. Simulations should obtain an empiric value, related to the crossing point of the drain's waveforms. Machado *et al.* [7] model the oscillator with native transistors operating at ultra-low voltages using the small-signal approximation.

This work presents the analysis of a special case of the cross-coupled oscillator without bias current and operating at low voltages. In the case analyzed, the transistors behave as ideal switches, being cutoff for a half period.

The rest of this work is organized as follows. Section II brings the working operation of the circuit and presents a proposal for the circuit model. In Section III the experimental setup for the characterization of the oscillator is shown. Experimental results and their analysis appear on Section IV. Conclusions and future works are given in Section V.

II. Operation of the Cross-Coupled Oscillator

The proposed oscillator is shown in Fig. 1. The working principle is described as follows. Suppose that, in a certain moment, M1 starts to conduct and, due to this, it presents a very small voltage drop between drain and source. This effect leads M2 to cutoff. Then the current that was passing by M2 suddenly stops. This causes a negative current step on L2. Combined with the parasitic components of the circuit (see Fig. 2), there is a sinusoidal oscillation at the drain of M2, reinforcing the conduction of M1. At the moment the voltage at M2 drain reaches zero V, M1 goes to cutoff. The current at the drain of M1 ceases rapidly, causing oscillation, now in the drain of M2. This leads M2 to conduction, presenting a very small drop between its drain and source and thus causing the cutoff of M1. M2 thus passes to replace M1 in the process, closing the cycle. Current and voltage waveforms are presented and discussed in Section IV.

For the analysis of the circuit, one should consider the circuit shown in Fig. 2. R1 and C1 are components from the gate of the transistor M2; R2 and C2 are components from the drain of the transistor M1, r is the series resistance of the inductor.

The inductor and the equivalent resistance and capacitance form an RLC branch, for which the following differential equation defines the current:

$$V_{DD} - L\frac{di}{dt} - (R + r)i - \frac{1}{C}\int idt = 0 \qquad (1)$$

The initial conditions are the current through the transistor when it switches off and the voltage over the inductor and its equivalent resistance at this moment:

$$L\frac{di(0)}{dt} + ri(0) = V_{DD} \qquad (2)$$

$$i(0) = I_M \qquad (3)$$

Combining the initial conditions of (2) and (3) and using (1), one can prove that the current in this circuit is given by the formula:

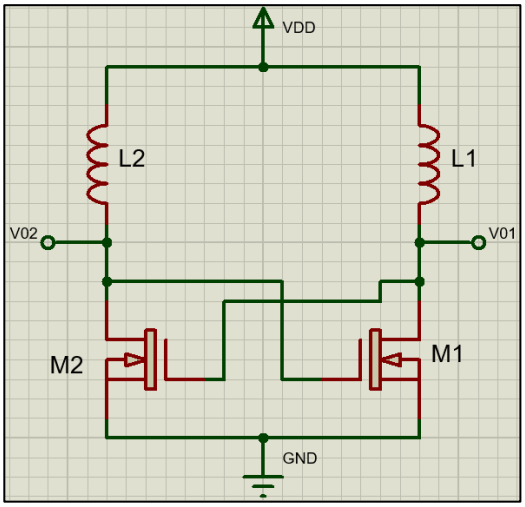

Fig.1. Schematic diagram of the oscillator

$$i(t) = I_0 e^{-\sigma_0 t} \cos(\omega_D t + \theta_I) \quad (4)$$

where:

$$\omega_D = \sqrt{\omega_0^2 - \sigma_0^2},\ \sigma_0 = \frac{R+r}{2L},\ \omega_0 = \frac{1}{\sqrt{LC}},$$
$$I_0 = \frac{I_M}{\cos\theta_I},\ I_M = \frac{V_{DD} T_F}{2L},$$
$$\theta_I = \tan^{-1}\left[-\left(\frac{2}{\omega_D T_F} + \frac{R-r}{2\omega_D L}\right)\right].$$

V_{DD} is the power supply; T_F is the period of oscillation; R and C are respectively the equivalent resistance and capacitance seen by the inductance. L1 and L2 are identical with value of L. During the conduction of the transistor, the current is a ramp due to the integration of the constant voltage V_{DD} over it. I_M is the peak current at the inductor, which occurs at the moment the transistor turns off (T_F/2).

According to Kirchhoff laws, the output voltage v_0 at the drain of any transistor is:

$$v_0(t) = V_{DD} - L\frac{di}{dt} - ri \quad (5)$$

Applying (4) on (5) and after some algebraic manipulation, one can prove that v_0 is given by the expression:

$$v_0 = V_{DD} + R_0 I_0 e^{-\sigma_0 t}[\sin(\omega_D t + \theta_I + \theta_D)] \quad (6)$$

where:

$$\theta_D = \tan^{-1}\left(\frac{R-r}{2\omega_D L}\right),\ R_0 = \sqrt{\frac{L}{C} - Rr}.$$

III. Experimental Setup

To perform the initial tests on the oscillator, the following measurement instruments were used:

- Waveform generator: Agilent 33250A
- DC power supply: Agilent E3631A
- Oscilloscope: Tektronix TDS 2014B
- LCR meter: Agilent E4980A
- Probes:
  - Tektronix CT-1 (current)
  - Tektronix P2220 (voltage)

The diagram of Fig. 1 represents the circuit as "ideal", which is not in accordance with reality. In fact, there are parasitic elements in the circuit, such as capacitances and resistances in both the terminals of the components and in the wires used.

The diagram of Fig. 2 represents how these parasitic elements could be comprehended in the circuit.

In order to calculate the values of these elements (resistances and capacitances), a test was conducted using the 33250A waveform generator, the oscilloscope with the current and voltage probes (the current probe is represented as an ammeter in the diagram), and two MOSFETs, simulating the circuit. Then, it was possible to find the values of R1, R2, C1 and C2. These values were found measuring the voltage and current amplitudes and the phase between them.

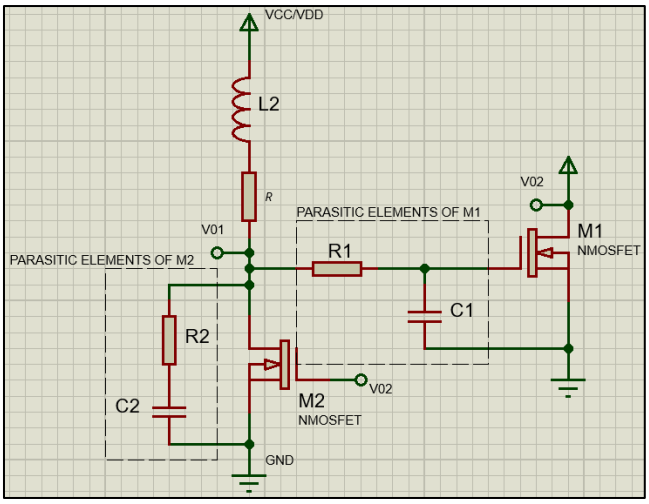

Fig.2. Parasitic elements in the circuit

TABLE I. Electrical Parameters of the Inductors

Parameter	Inductor 1	Inductor 2	Inductor 3
Inductance	3.28 µH	3.31 µH	3.32 µH
Resistance	230 mΩ	280 mΩ	360 mΩ

To determine the resistance and inductance, the characterization of three inductors available for L1 and L2 was also made. For this, a protoboard and one inductor at a time were used, along with the E4980A RLC meter. The results obtained for the frequency of 2.0 MHz are shown in Table I. Therefore, it was possible to determine an average inductance and resistance of 3.30 µH and 290 mΩ respectively.

IV. Experimental Results

The circuit was assembled using BSH103 transistors from NXP due to their high current capacity and low threshold voltage. Characterization of parasitic components using the method above detailed found C=731 pF and R=18.0 Ω. The circuit starts oscillating with 639 mV.

Current and voltage waveforms at a 2.0 V power supply are shown in Figs. 4, 5 and 6. Voltage waveforms are quite close to sinusoids. Each transistor goes to cutoff during half period.

A significant ringing is observed in the waveforms. This effect is caused by the approximation of the drain voltage to the threshold voltage V_{TH} (about 1.06 V for the BSH103). In this situation, when the waveform at the drain of one transistor, say M1, is getting close to V_{TH}, it starts to cut the current of the other one, M2. When this happens, the voltage at the drain of M2 starts to rise, leading M1 to rise its current and its drain voltage, since it is now in the weak to moderate inversion level.

The rise in the drain voltage of M1 leads M2 to revert its path to cutoff. The current of M2 increases but, in this case, the voltage at the drain lowers since it is entering in the strong inversion level. This effect is in opposite direction of the previous one, leading the current and drain voltage of M1 to lower. This mutual interaction explains the ringing of the currents.

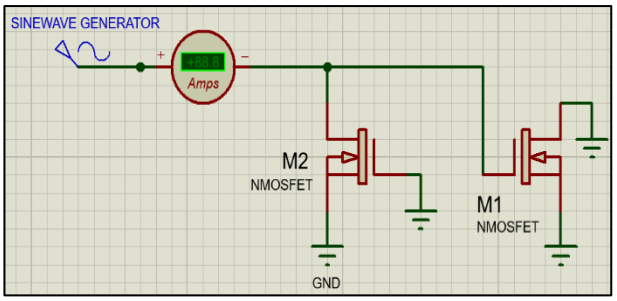

Fig.3. Circuit used to find parasitic elements

Its duration is determined by internal and parasitic components. The current ringing also influences the voltage waveforms, as can be seen in the figures.

Fig. 4 brings the current waveform at the gate of M1. Neglecting the previously explained ringing, it is possible to see a sinusoidal shape in this current, compatible with the hypothesis that the voltage at drain is also a sinusoidal waveform. During the cutoff period, there is no current since the drain voltage is constant.

Fig. 5 shows the current waveform in L1. One can see a sinusoidal waveform in the cutoff period of M1, again confirming that the voltage waveform at the drain is sinusoidal. During the conduction of M1, the current is a ramp, because of the integration of a constant voltage at the inductor.

Fig. 6 shows the waveform of the current in the drain of M1. This transistor absorbs the current through the inductor when it is conducting. The current suffers an abrupt cutoff, as previewed by the theory. The on resistance (r_{on}) is so low that it is not possible to see any alteration in the drain to source voltage.

In order to obtain T_F, it is necessary to find the period where v_0 nulls, which corresponds to $T_F/2$. Eq. (6) does not have an analytical solution, so a numerical one should be provided. Applying the values from the characterization of the circuit, the oscillation frequency $f_F = 1/T_F$ found by the software MATLAB is 2.650 MHz. When compared to the experimental frequency (2.600 MHz), there is a deviation of 1.9 %. The experimental frequency lowers about 40 kHz/V with the increase of the power supply. This drift is caused by the decrease of the superposition period of the drain waveforms, which causes a slight variation in the period of oscillation. This effect is not predicted by the proposed theory, which defines a constant oscillation frequency. Fig. 7 shows both curves as functions of the power supply.

Fig. 8 illustrates the peak amplitude of the drain voltage as a function of the power supply. Theoretical values are about 37 % higher than the experimental ones. This can be explained by the transition of the transistors through subthreshold region and by the fact that the voltage at the gate is not a voltage step, but a ramp. In addition, the transistors have a nonzero resistance. These effects lead the maximum current I_M to be lower than that predicted by the theory, since they delay and decrease the conduction of the transistor.

Figure 9 shows a comparison between the theoretical and experimental waveforms, normalized by the peak value of each waveform's data. They are very similar, showing that the approach represents the real behavior of the circuit.

V. Conclusions and Future Works

A low-voltage cross-coupled oscillator was assembled and analyzed. An explanation to the working principle was presented. A preliminary model to the special case when transistors are considered as ideal switches was proposed.

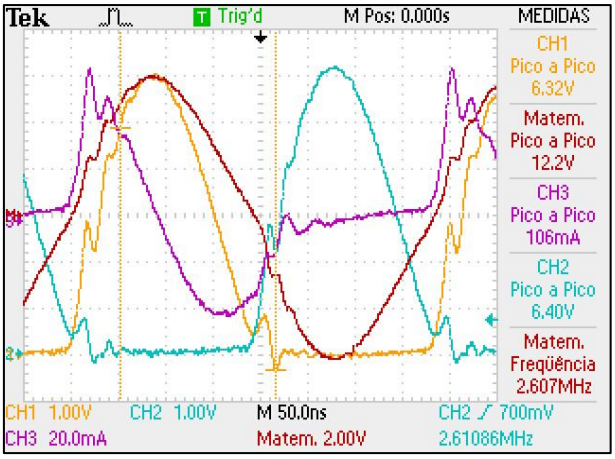

Fig.4. Waveforms at the oscillator. CH1: voltage at the drain of M1, CH2: voltage at the gate of M1, CH3: current at the gate of M1, Mathematic: differential voltage between the drains

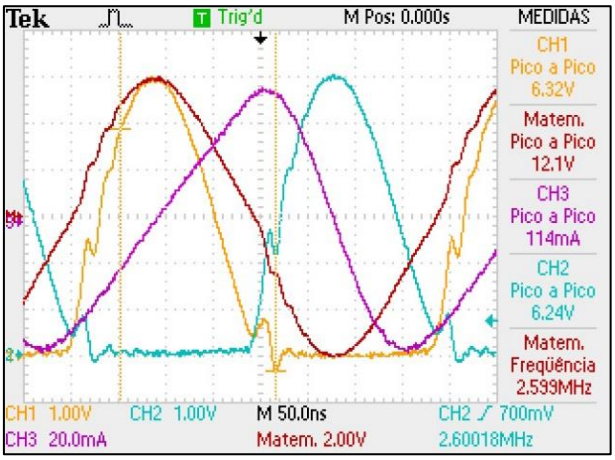

Fig.5. Waveforms at the oscillator. CH1: voltage at the drain of M1, CH2: voltage at the gate of M1, CH3: current at L1, Mathematic: differential voltage between the drains

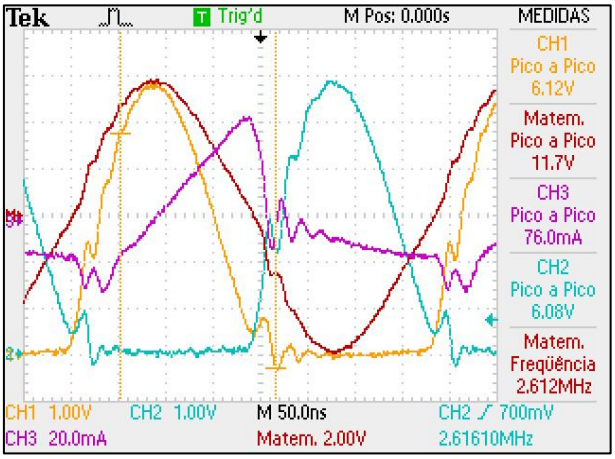

Fig.6. Waveforms at the oscillator. CH1: voltage at the drain of M1, CH2: voltage at the gate of M1, CH3: current at the drain of M1, Mathematic: differential voltage between the drains

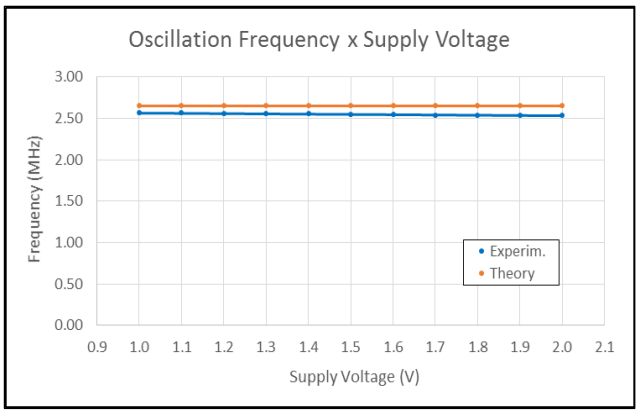

Fig.7. Theoretical and experimental oscillation frequencies as functions of the power supply

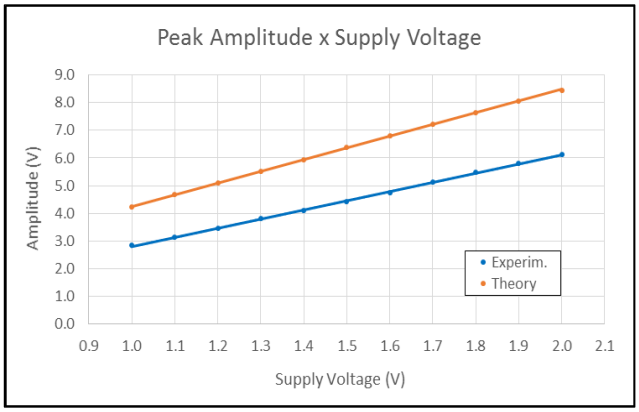

Fig.8. Theoretical and experimental peak amplitudes as functions of the power supply

The theoretical result in the oscillation frequency is quite close to the experimental one. In order to get a more faithful model for the peak amplitude, it is necessary to consider the complex relation between currents and voltages in the subthreshold region and the slower transition of the gate voltage. This is a topic for future research.

The modeling can be applied to circuits with different transistors and can accurately preview the oscillation frequency once the parasitic resistance and capacitance can be measured or predicted by design.

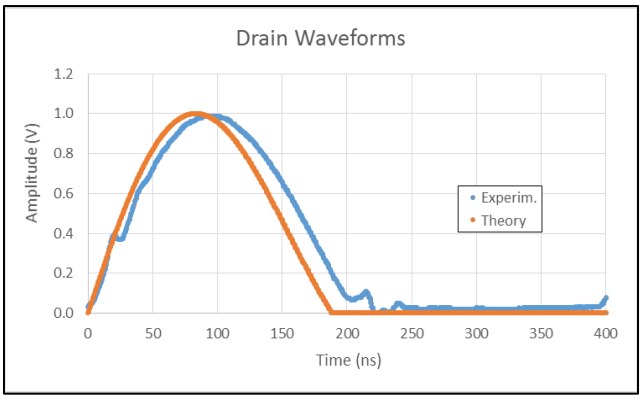

Fig.9. Drain waveforms, normalized by the peak value in order to show the similarity between the theoretical and experimental curves

ACKNOWLEDGMENT

The authors would like to thank CNPq by the scholarship of R. G. Ono.

REFERENCES

[1] J. Rogers and C. Plett, Radio Frequency Integrated Circuit Design, Artech House, 2003, chap. 8.

[2] A. Buonomo and A. Lo Schiavo, “Large-signal analysis of CMOS – LC VCOs”. IEEE ECCTD, May 2007, pp. 994–997.

[3] A. Buonomo and A. Lo Schiavo, “Finding the tuning curve of a CMOS – LC VCO”, IEEE Trans. Circuits Syst. II, Express Briefs, vol. 55, no. 9, pp. 887–891, September 2008.

[4] A. Buonomo and C. Di Bello, “Asymptotic formulas in nearly sinusoidal nonlinear oscillators”, IEEE Trans. Circ. Systems I: Fundamental Theory e Applications, vol. 43, no. 12, pp. 953-963, December 1996.

[5] X. Ge, M. Arcak and K. N. Salama, “Nonlinear analysis of ring oscillator and cross-coupled oscillator circuits”, Dynamics of Continuous, Discrete and Impulsive Systems Series B: Applications and Algorithms [online]: http://hdl.handle.net/10754/247352.

[6] M. Daliri and M. Maymandi-Nejad, “Analytical model for CMOS cross-coupled LC-tank oscillator”, IET Circuits Devices Syst., pp. 1–9, 2013.

[7] M. B. Machado, M. C. Schneider and C. Galup-Montoro, “On the minimum supply voltage for MOSFET oscillators,” IEEE Trans. Circ. Systems I: Reg. Papers, vol. 62, no. 2, pp.347-357, February 2014.